physical characteristics of said first portion;

means for generating, in response to said dividing, an approximate mathematical model of said second portion of said system, said model being based upon hierarchical analysis of said remaining portion; and

using both said physically-accurate description and said approximate model to simulate the operation of said system.

REMARKS

This amendment is filed in response to the FINAL Office Action mailed on 2 December 2003, and in the Continued Prosecution Application (CPA) filed on even date herewith. All objections and rejections are respectfully traversed.

Claims 1-17 are pending.

Claims 13-17 were added to better claim the invention.

At paragraph 2 of the Office Action claims 1-12 were rejected under 35 U.S.C. § 112, first paragraph.

In paragraph 2.2 regarding claims 1-4, and 9-12, it is asserted that the Specification "while being enabling for generating an approximate model of a remaining portion of a system, does not reasonably provide enablement for generating an approximate mathematical model of a remaining portion of a system."

Generation of a "approximate mathematical model" of a portion of the system is disclosed in the Specification at the following places:

In the "Brief Description of Related Prior Art", beginning on page 2,

at page 4 beginning at line 15: "In HA, rather than basing the simulation of the design's timing operation upon the design's actual physical characteristics, the simulation is instead based upon approximate or estimated mathematical models of operation of portions of the design.";

at page 4 beginning at line 17: "approximate or estimated mathematical models";

at page 4 beginning at line 18: "That is, respective mathematical models are generated for respective functional blocks comprising the design which may be used to estimate the timing

operation of the design. The design's timing operation is then simulated using these approximate models.";

in the "DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS"

at page 12 beginning at line 2: "In essence, functions 82, 84, 86 are mathematical functional abstractions, based upon the physical characteristics of the proposed design 100 in the databases 46, 48, that may be used to estimate the overall timing operations of module 65, connection 70, and module 67, respectively, as a functions of the inputs 50, 80 and clock signals CLK provided thereto.";

at page 12 beginning at line 6: "function 82 essentially is an approximate mathematical model of the overall timing operation of the module 65";

at page 12 beginning at line 10: "Similarly, function 84 essentially is an approximate mathematical model of the overall timing operation of the connection 70";

at page 12 beginning at line 12: "Also similarly, function 86 essentially is an approximate mathematical model of the overall timing operation of the module 67 that is based upon, but is not itself, an accurate description of the physical characteristics of the circuits, networks, etc. comprised in module 67 or blocks 72, 74, 76, comprised in module 67."; and

at page 13 beginning at line 12: "The simulation generated by the engine 32' inherently includes approximation error, since it is based upon the approximate mathematical models 82, 84, 86 of the HA model 150."

Applicant respectfully urges that the above disclosures of the use of "approximate mathematical" functions or models for analysis in the claimed invention meet all requirements of applicable law and rules, including 35 U.S.C. § 112, first paragraph. Particularly, the use at page 4 in the "Brief Description of Related Prior Art" section of the Specification indicates that use in the "hierarchical analysis (HA)" technique is known in the art, and so a person of ordinary skill in the art of designing computer chips and doing analysis on the chips will be familiar with the HA method.

Accordingly, Applicant respectfully urges that no further disclosure in the present Application for United States Patent of the well known HA method is required by Law or Rule.

Further, Applicant identifies the use of "mathematical models" and "approximate mathematical methods" in practice of the claimed invention at pages 12 and 13 of the Specification, as detailed hereinabove. Applicant respectfully urges that these disclosures of the use of "approximate mathematical models" at pages 12 and 13 sufficiently disclose to a person of ordinary skill in the art of computer chip design and analysis of the chips so that he can practice the invention without undue experimentation.

At paragraph 2.3 of the Office Action claims 5-8 were rejected under 35 U.S.C. §112, first paragraph. It is asserted that "because the Specification, while being enabling for estimating operation of system using hierarchical analysis functions, does not reasonably provide enablement for estimating operation of system using hierarchical analysis mathematical functions."

Again, Applicant respectfully urges that the disclosures of the use of "mathematical functions" at pages 4, 12, and 13 of the Specification adequately discloses the use of these mathematical functions, so that a person of ordinary skill in the art of computer chip design and analysis of the chips can practice the invention without undue experimentation.

At paragraph 2.4 of the Office Action, the Examiner requests for an indication in the Specification where the use of "mathematical" functions is adequately disclosed.

Applicant respectfully urges that the disclosure of the use of "mathematical" functions explained hereinabove at pages 4, 12, and 13 of the Specification adequately disclose the use of "mathematical" functions as claimed herein.

At paragraph 3 of the Office Action, including paragraphs 3.1, 3.2, and 3.4, claims 1-12 were rejected under 35 U.S.C. § 112, second paragraph.

It is asserted that the term "approximate mathematical model" is not defined by either claim 1 or claim 9.

Applicant respectfully urges that the use of the term "approximate mathematical model" in HA analysis in the "prior art" section of the present specification adequately explains to a person of ordinary skill in the art of computer chip design, and analysis of the design, how to practice the invention without undue experimentation.

Accordingly, Applicant respectfully urges that the foundation in the Specification of the use of the HA method and the use of the term of art "approximate mathematical models" at page 4 of the Specification is adequate to use the term of art in a claim.

Also, it is urged that the term "hierarchical analysis mathematical functions" in claim 5 is a relative term which renders the claim indefinite.

Applicant respectfully urges that the term "hierarchical analysis mathematical functions" is a term which those skilled in the art of computer chip design are familiar with, as they are familiar with the HA design model, as set out in the "Prior Art" section of the Specification.

Accordingly, Applicant respectfully urges that the use of the term of art "hierarchical analysis mathematical functions" is adequately disclosed so that a person of ordinary skill in

the art of computer chip design, and analysis of the design, can practice the invention without undue experimentation.

At paragraph 4 (4.1, 4.2, 4.3, 4.4, 4.5) of the Office Action, claims 1-12 were rejected under 35 U.S.C. § 102 as being anticipated by Shepard et al., "Design Methodology for the S/390 Parallel Enterprise Server G4 Microprocessors", hereinafter "Shepard".

As set out in representative claim 1, the present invention comprises in part:

> 1. A computerized method for use in simulating an operation of an electronic system, said method being carried out using a computer system, said method comprising the steps of:
>
> ***generating a physically-accurate description of a first portion of said system, said physically-accurate description comprising actual physical characteristics of said first portion***;
>
> generating an ***approximate mathematical model*** of a remaining portion of said system, said model being based upon hierarchical analysis of said remaining portion; and
>
> ***using both said physically-accurate description and said approximate model to simulate the operation of said system***.

Shepard discloses a design methodology used in the design of a microprocessor, including timing analysis of the microprocessor. The tool (computer program) Pathmill was used to analyze abstractions based on netlists to produce black boxes (no internal latch points) or gray boxes (internal latch points are defined), pages 529-530. The tool EinsTimer

was used to analyze black or gray boxes connected by "pi-model residue global models described in Section 4", page 530. Section 4 of Shepard, pages 523-526 describes an approximate model for interconnections based on various approximations to internal resistances, capacitances, and inductances. Shepard uses EinsTimer to combine his black or gray boxes using his pi-model residue approximation.

Applicant respectfully urges that the presently claimed invention combines ***generating a physically-accurate description of a first portion of said system, said physically-accurate description comprising actual physical characteristics of said first portion*** with a an "***approximate mathematical model***" for a second part of the circuit, and then ***using both said physically-accurate description and said approximate model to simulate the operation of said system***. Shepard simply uses two levels of approximation, first his approximate black or gray boxes, and then he combines them using his pi-model for interconnection of his boxes. In sharp contrast, Applicant uses a ***physically-accurate description*** for a first part of the circuit, and an ***approximate mathematical model*** for a second part of the circuit, and then combines the approximation with the physically accurate description to do analysis of the entire circuit.

Again, Applicant uses a ***physically-accurate description*** for a first part of his circuit for analysis. Applicant then uses an ***approximate mathematical model*** for a second part of the circuit for analysis. Applicant then combines his physically accurate description for a first part of his circuit and his approximate mathematical model for the second part of the cir-

cuit to do a complete analysis of his circuit. In contrast, Shepard combines two approximate methods, first the Pathmill tool to produce boxes (black or gray), and secondly his pi-model to plug his boxes together in the EinsTimer computer program.

Accordingly, Applicant respectfully urges that the Shepard document is legally precluded from anticipating the presently claimed invention under 35 U.S.C. § 102 because of the absence from Shepard of Applicant's claimed novel use of a ***physically-accurate description*** for a first part of his circuit combined with an ***approximate mathematical model*** to simulate operation of his entire system.

At paragraphs 5 and 6 of the Office Action the Applicant's earlier argument is summarized, and it is noted that the Shepard document is now cited rather than the McDonald reference. As set forth above with reference to representative claim 1, Applicant respectfully urges that the Shepard document does not disclose Applicant's claimed novel combination of a ***physically-accurate description*** for a first part of the circuit combined with an ***approximate mathematical model*** to simulate operation of the entire system. Shepard does not disclose use of a physically accurate description, Shepard discloses use of a pi-model to interconnect the Pathmill boxes.

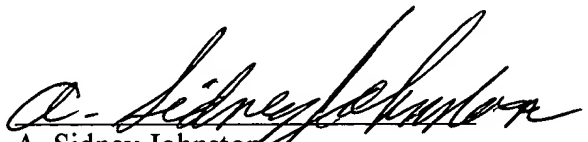
All independent claims are believed to be in condition for allowance.

All dependent claims are believed to be dependent from allowable independent claims, and therefore in condition for allowance.

Favorable action is respectfully solicited.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,



A. Sidney Johnston
Reg. No. 29,548
CESARI AND MCKENNA, LLP
88 Black Falcon Avenue
Boston, MA 02210-2414
(617) 951-2500